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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/815,548	03/22/2001	Michael Stephen Floyd	AUS920010017US1	6460

7590 03/18/2005

Kelly K. Kordzik
100 Congress Avenue, Suite 800
Austin, TX 78701

EXAMINER	
LE, DIEU MINH T	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 03/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/815,548	FLOYD ET AL.	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is response to the communication filed on 01/21/05 in application 09/815,548.

2. Claims 1-33 are presented for examination.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in

order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-33 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Anderson et al (US Patent 6,393,594 hereafter referred to as Anderson) in view of Floyd et al (US 2002/0129309 A1 hereafter referred to as Floyd).

As per claim 1:

Anderson substantially teaches the invention. Anderson teaches:

- A method for debugging (i.e., testing) a system [fig. 3, abstract, col. 1, lines 5-14; col. 2, lines 36-47]; comprising:

- 1)coupling first signals [col. 10, lines 15-17] to a re-writeable trace array [col. 5, lines 45-49], said trace array having M storage locations, said M storage locations [col. 6, lines 31-40] having corresponding M storage addresses from a starting address to an ending address [col. 7, lines 10-40];

- 2)generating a first event sequence signal in response to a first sequence of occurrences of a first event signal [col. 5, lines 30 through col. 6, lines 18];

- 3)starting, in response to said first event sequence signal, a process of storing states of said first signals sequentially in said trace array at locations beginning at said starting address and proceeding sequentially to said ending address, [col. 5, lines 30 through col. 6, lines 18];

- 4)generating a second event sequence signal (i.e., error signal) [col. 5, lines 30-49] in response to a second sequence

of occurrences of said first event signal [col. 5, lines 50 through col. 6, lines 18];

- 5)stopping said process of storing states of said first signals in said trace array in response to said second event sequence signal (i.e., error signal) [col. 4, lines 18-39; col. 5, lines 30-49];

- 6)repeating steps 2) through 5) unless stopped by a second event signal (i.e., error signal) [fig. 7-8, col. 4, lines 18-39; col. 5, lines 30-49].

Anderson does not explicitly teach:

- process of storing states of said first signals wrapping back to said starting address when said ending address is exceeded.

However, Anderson does disclose capability of:

- A method and system for testing an integrated circuit having trace array [abstract, fig. 5, col. 1, lines 5-15] comprising:

- a connectivity among trace array, register, controller, MISR trace select, comparator, error detection device, etc… [fig. 3, col. 5, lines 23-49];

- ***test engine controlling the data between pattern generator and checker via sequencing of data including run function, stop on error function, looping ability*** [col. 4, lines 29-39].

In addition, Floyd explicitly teaches:

- A method and system for triggering a debugging unit having trace array and logic analyzer [fig. 2, abstract, col. 1, par. 0002]
comprising:

- ***a sub-sequencing signaling of first, second, third states, etc… and back to first states via debugging operation*** [col. 4, claims 4 and col. 5, claims 10].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention was made to:

+ first, realizing Anderson's ***test engine controlling the data between pattern generator and checker via sequencing of data including run function, stop on error function, looping ability*** as being the process of storing states of said first signals wrapping back to said starting address when said ending address is exceeded as claimed by Applicant. This is because Anderson explicitly deals with the processor and trace memory testing and debugging process. Therefore, the process of storing, testing, signaling of starting and ending of trace memory addresses as well as locations including looping back or wrapping back feature are fully performed therein by Anderson in order to ensure the data in trace memory process correctly.

+ second, by applying the ***a sub-sequencing signaling of first, second, third states, etc… and back to first states via debugging operation*** as taught by Floyd in conjunction with the Anderson's method and system for testing an integrated circuit having trace array; the computer system, more specifically the processor within the integrated circuit can be tested, debugged, detected, traced, and corrected any failures in maximizing the

data accessing, data registering, data shifting via data controlling and tracing environment.

One of ordinary skill in the art would have been motivated to do so to provide the processing debugging system with mechanism to improve data availability and controlling in ensuring data registered, addressed, shifted, loop back properly with the trace memory array. That is by utilizing this approach, any error or failure occurred in the trace array can be identified, detected, corrected and traced via data tracing control capability. This would enhance the processor's operation process.

As per claim 2:

Anderson further teaches:

- storing an event storage address in response to receipt of said first event sequence signal, said second event sequence signal or said second event signal, said event storage address corresponding to a storage address of sub-array K which is storing states of said first signals when said first event sequence signal, said second event sequence signal or said second event signal occurred [col. 7, lines 31-40 and col. 8, lines 34-50];

In addition, Floyd explicitly teaches:

- A method and system for triggering a debugging unit having trace array and logic analyzer [fig. 2, abstract, col. 1, par. 0002]

comprising:

- ***storing data within trace array, processing and analyzing data for its debugging process*** [col. 3, par 0036-0040].

As per claim 3:

Anderson further teaches:

- reading stored states of said first signals from selected storage addresses of said trace array; and analyzing said stored states of said first signals to debug or analyze said system [col. 5, lines 30 through col. 6, lines 18].

As per claim 4:

Anderson further teaches:

- stored event storage addresses is compared to a read storage address of said trace array during reading said stored states of said first signals, a comparison match of said stored event storage address to said read storage address corresponding to event or error states of said first signals [abstract, col. 7, lines 31-40 and col. 10, lines 61-65].

In addition, Floyd explicitly teaches:

- A method and system for triggering a debugging unit having trace array and logic analyzer [fig. 2, abstract, col. 1, par. 0002]

comprising:

- ***storing data within trace array, processing and analyzing data for its debugging process*** [col. 3, par 0036-0040].

As per claims 5-6:

Anderson further teaches:

- logic circuits in a very large scale integrated circuit (VLSI) chip [col. 1, lines 10-14];

- re-writeable trace array is included within said VLSI chip [fig. 7, col. 1, lines 10-14 and col. 8, lines 34-60].

As per claim 7:

Anderson further teaches:

- first and second event signals are logic combinations of circuit states occurring within said system (i.e., first signaling and error signaling) [fig. 3, col. 5, lines 23-49].

As per claim 8:

Anderson further teaches:

- a storage address of said trace array, corresponding to said first event sequence signal, said second event sequence signal or said second event signal, is saved [fig. 3-4, col. 6, lines 19-64].

As per claims 9-11:

Anderson further teaches:

- first sequence of occurrences of said first event signal comprises a next sequential first event signal following a start signal [fig. 3-4, col. 5, lines 23 through col. 6, lines 19-64];

- second sequence of occurrences of said first event signal comprises a next sequential first event signal following said first event sequence signal [fig. 3-4, col. 5, lines 23 through col. 6, lines 19-64];

In addition, Floyd explicitly teaches:

- A method and system for triggering a debugging unit having trace array and logic analyzer [fig. 2, abstract, col. 1, par. 0002]

comprising:

- storing data within trace array, processing and analyzing data for its debugging process [col. 3, par 0036-0040].

- first, second, third signaling and first, second, third operating states performing sequentially in supporting the debugging of the computer processing system [col. 1, par. 0007-0012].

As per claims 12-22:

Due to the similarity of claims 12-22 to claim 1-11 except for an apparatus for debugging a system comprising a first signal to a re-writeable trace array, first event sequence signal, a second event sequence signal, etc… instead of a method for debugging a system comprising a first signal to a re-writeable trace array, first event sequence signal, a second event sequence signal, etc…; therefore, these claims are also rejected under the same rationale applied against claims 1-11. **In addition, all of the limitations have been noted in the rejection as per claims 1-11.**

As per claims 23-33:

Due to the similarity of claims 23-33 to claim 1-11 except for a data processing system comprising a first signal to a re-writeable trace array, first event sequence signal, a second event sequence signal, etc… instead of a method for debugging a system comprising a first signal to a re-writeable trace array, first event sequence signal, a second event sequence signal, etc…; therefore, these claims are also rejected under the same rationale applied against claims 1-11. **In addition, all of the limitations have been noted in the rejection as per claims 1-11. Floyd explicitly teaches CPU, RAM, ROM, I/O adapter, a bus system, etc… [fig. 1].**

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. A shortened statutory period for response to this action is set to expired THREE (3) months, ZERO days from the date of this letter. Failure to respond within the period for response will cause the application to be abandoned. 35 U.S.C. 133.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (571) 272-3660. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The Tech Center 2100 phone number is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DIEU-MINH THAI LE
PRIMARY EXAMINER
ART UNIT 2114

DML
3/16/05